Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.090”**

**G**

**SOURCE**

**.115”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .021” X .022”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .090” X .115” DATE: 6/5/23**

**MFG: INT’L RECTIFIER THICKNESS .010” P/N: IRFC234**

**DG 10.1.2**

#### Rev B, 7/1